

MODEL 3380P

KEY FEATURES

- 50/100 MHz clock rate
- 50/100 Mbps data rate
- 512 digital I/O pins (channels)
(Max 576 digital I/O pins)
- Up to 512 sites parallel testing
- 32/64/128M pattern memory
- 16M capture memory per pin
- Various VI source
- Flexible HW-architecture
(Interchangeable I/O, VI, ADDA)
- Real parallel trim/match function
- Time & Frequency Measurement Unit
(TFMU)
- AD/DA test (16/24 bits option)
- SCAN test option (max. 2G M/chain)
- ALPG test option for embedded memory
- STDF tools support
- Test program/pattern converter
(J750, D10, S50, E320, SC312, V7, TRI-6836)
- Direct mount probe card is compatible
with 3360P/3380D direct mount probe
card (only 256pins)
- Cable mount DUT card is compatible with
3360D/3360P/3380D cable mount DUT
card (FT/CP)
- CRAFT C/C++ programming language
Software is compatible with 3360/3360P
- User friendly Windows 7 environment

VLSI TEST SYSTEM MODEL 3380P

In order to cope with the IC testing trend of high-speed, numerous pins and complex functions in the future, the newest generation of Chroma's VLSI test systems, 3380D/3380P/3380, have adopted a more flexible architecture with higher integration density and powerful functions.

The 3380D/3380P/3380 test systems have 4 wires HD VI source and any-pins-to-any-site

high parallel test (multi-sites test) functions (512 I/O pins to test 512 ICs in parallel) that can meet the upcoming higher IC testing demands.

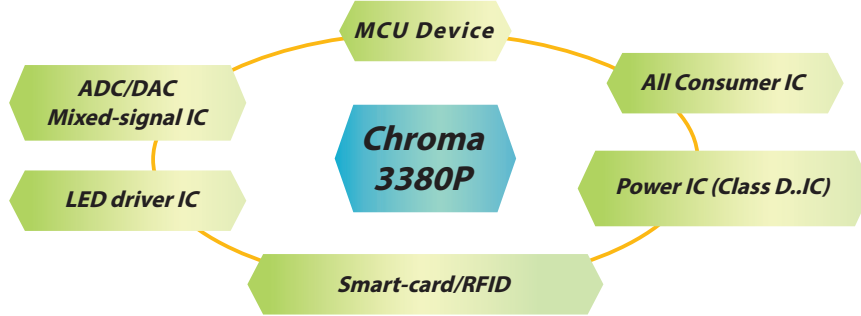
The test system 3380P also has built in all-in-one design (for test head only) to provide a small footprint/clear power ATE to become a very competitive price/performance ratio test system.



Chroma

RICH FUNCTIONS AND WIDE COVERAGE

Logic, MCU, ADDA (Mixed-signal) ; Power, LED driver, Class D ; SCAN, ALPG, Match and etc.

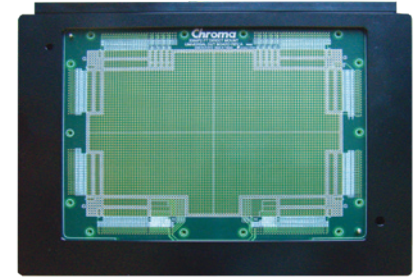


SPECIFICATIONS

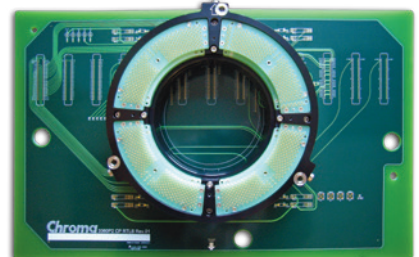
Model	3380P
Clock Rate	50/100 MHz
Data Rate	50/100 Mbps
Pin Channels	512 pins (Max. 576 pins)
Pattern Memory	32M(S) / 64 & 128M (option)
Capture Memory	16M per pin (50 MHz)
Parallel Testing Capability	512 DUTs
EPA	± 500ps
Resource Per Pin Architecture	Yes
VI source	8CH : MXDPS 16CH : MLDPS-16(S) / MXUVI / MXREF 32CH : MLDPS
PMU(± 48V, ± 100 mA)	16 Channels /board
HV-Pins driver (+5.9V to +13.5V)	4 channels /board
PPMU (-2V~+ 6V, ± 32 mA)	Per pin (FIMV/FVMI)
Programmable Active Load (± 12 mA)	Per pin
TFMU (Time/Freq Measure Unit : Max. 400 MHz)	Per pin
Free-run Clock (Max. 200 MHz)	Per pin
Windows Environment	Window 7
Programming Language	C/C++
Test Option	Specification
AD/DA Converter Test Option (MXAWI/MXAWI2)	4 AWG / 4 DIG (16 bits)
Mixed-signal Test Option (NI PXI)	24 bits, 200MS/s
MXUVI (DPS ± 12V, ± 1A, CG ± 4A)	16 channels /board
MXDPS (DPS ± 16V, ± 2A)	8 channels /board
MXREF (DPS ± 48V, ± 250mA, CG ± 1A)	16 channels /board
MLDPS (DPS +12V/± 500mA, ± 6V/± 1A, CG max. ± 32A)	32 channels /board
SCAN Option	1G bits/chain (2G option)
ALPG Memory Test Option	16X, 16Y, 16D/board
System and Dimension	
Power Consumption	Max. 3KVA
Only Test Head	W640 x D470 x H639 mm (Max.100Kg)

* **Note 1:** "Direct-Mount" as Standard, "Cable-Mount" as Option

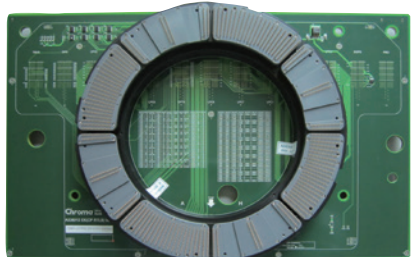
CP/FT DIRECT/CABLE MOUNT



3380P FT Direct-mount



3380P G-type Direct-mount



3380P J-type Direct-mount

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